CLAIMS

We claim:

1. A method, comprising:

creating at least one interlayer via by etching a portion of an interlevel dielectric (ILD) layer and a portion of a ferroelectric polymer layer of a ferroelectric polymer die down to a first metal layer;

filling the at least one interlayer via with a fill metal by depositing the fill metal in the vias through an electroless plating process; and

depositing a second metal layer over the ILD layer and the at least one filled interlayer via.

2. The method of claim 1, wherein filling the vias with the fill metal comprises depositing the fill metal to a level where the top of the fill metal is below the top of the ILD layer.

3. The method of claim 1, wherein to fill the vias with the fill metal comprises:

filling the at least one interlayer via to a level where the top off the fill metal is above the top of the ILD layer; and

polishing the fill metal until the top of the fill metal is level with the top the ILD layer.

4. The method of claim 1, wherein the fill metal is selected from a list consisting essentially of nickel (Ni), cobalt (Co), chromium (Cr), iron (Fe), tin (Sn), copper (Cu), silver (Ag), gold (Au), palladium (Pd), platinum (Pt), ruthenium

(Ru), rhodium (Rh), iridium (Ir), osmium (Os), and metal alloys thereof, and alloys with metalloids consisting essentially of phosphorous (P), boron (B), nitrogen (N), and silicon (Si).

5. The method of claim 1, wherein the electroless plating process comprises:

activating the first metal layer by placing the ferroelectric polymer stack in a metal activation solution;

rinsing the stack with ultra pure water (UPW);

depositing the fill metal in the at least one interlayer via by placing the ferroelectric polymer die in a metal plating solution having a predefined concentration of metal and heated to a predefined temperature;

rinsing the ferroelectric polymer die in UPW; and

drying the ferroelectric polymer die.

6. The method of claim 1, wherein the first metal layer has a predetermined thickness in the range of 20 nanometers to 100 nanometers.

7. The method of claim 6, wherein the ferroelectric polymer layer has a predetermined thickness in the range of 40 nanometers to 200 nanometers.

8. The method of claim 7, wherein the ILD layer has a predetermined thickness of approximately 200 - 500 nanometers.

9. The method of claim 1, wherein the second metal layer has a predetermined thickness in the range of 20 nanometers to 100 nanometers.

10. The method of claim 6, wherein the activation solution is a palladium chloride ($PdCl_2$) solution having a concentration of about 0.2 - 2.0 grams per liter.

11. The method of claim 6, wherein the metal plating solution is a nickel chloride ($NiCl_2 \cdot 6H20$) solution having a concentration of approximately 20 – 40 grams per liter.

12. The method of claim 8, wherein the width of the open area in the photoresist is approximately 1 to 1.5 times the thickness of the combined thickness of the ILD layer and the ferroelectric polymer layer.

13. A ferroelectric polymer die, comprising:

a silicon (Si) substrate;

an oxide thermal insulation layer on top of the Si substrate;

a first metal layer on top of the oxide layer;

a ferroelectric polymer layer on top of the first metal layer;

an interlevel dielectric (ILD) layer on top of the ferroelectric polymer layer;

a second metal layer having on top of the ILD layer; and

a via metal fill plug passing through the ILD layer and the ferroelectric polymer layer to electrically connect the first metal layer to the second metal layer.

14. The ferroelectric polymer die of claim 13, wherein the via metal fill plug is below the top of the ILD layer.

15. The ferroelectric polymer die of claim 14, wherein the second metal layer comprises a step at the via metal fill plug.

16. The ferroelectric polymer die of claim 15, wherein the second metal layer has a thickness in the range of 20 nanometers to 100 nanometers.

17. The ferroelectric polymer die of claim 16, wherein the step is less than one third the thickness of the second metal layer.

18. The ferroelectric polymer die of claim 13, wherein the via metal fill metal plug is coplanar with the ILD layer.

19. The ferroelectric polymer die of claim 18, wherein the second metal layer has a thickness in the range of 20 nanometers to 100 nanometers.

20. The ferroelectric polymer die of claim 13, wherein the interlayer via plug comprises a metal selected from a list consisting essentially of nickel (Ni), cobalt (Co), chromium (Cr), iron (Fe), tin (Sn), copper (Cu), silver (Ag), gold (Au), palladium (Pd), platinum (Pt), ruthenium (Ru), rhodium (Rh), iridium (Ir), osmium (Os), and metal alloys thereof, and alloys with metalloids consisting essentially of phosphorous (P), boron (B), nitrogen (N), and silicon (Si).

21. The ferroelectric polymer die of claim 20, wherein the interlayer via plug is formed by an electroless plating process.

22. A ferroelectric polymer memory die, comprising:

a silicon (Si) substrate;

an oxide thermal insulation layer on top of the Si substrate;

a plurality of metallization layers stacked on the oxide layer, wherein each metallization layer comprises:

a first metal layer;

a ferroelectric polymer layer on top of the first metal layer;

an interlevel dielectric (ILD) layer on top of the ferroelectric polymer layer; and

a second metal layer on top of the ILD layer; and

at least one via metal fill plug passing through the ILD layer and the ferroelectric polymer layer to electrically connect the first metal layer to the second metal layer.

23. The ferroelectric polymer die of claim 22, wherein the via metal fill plug is below the top of the ILD layer.

24. The ferroelectric polymer die of claim 22, wherein the second metal layer comprises a step at the via metal fill plug.

25. The ferroelectric polymer die of claim 22, wherein the interlayer via plug comprises a metal selected from a list consisting essentially of nickel (Ni), cobalt (Co), chromium (Cr), iron (Fe), tin (Sn), copper (Cu), silver (Ag), gold (Au), palladium (Pd), platinum (Pt), ruthenium (Ru), rhodium (Rh), iridium (Ir), osmium (Os), and metal alloys thereof, and alloys with metalloids consisting essentially of phosphorous (P), boron (B), nitrogen (N), and silicon (Si).